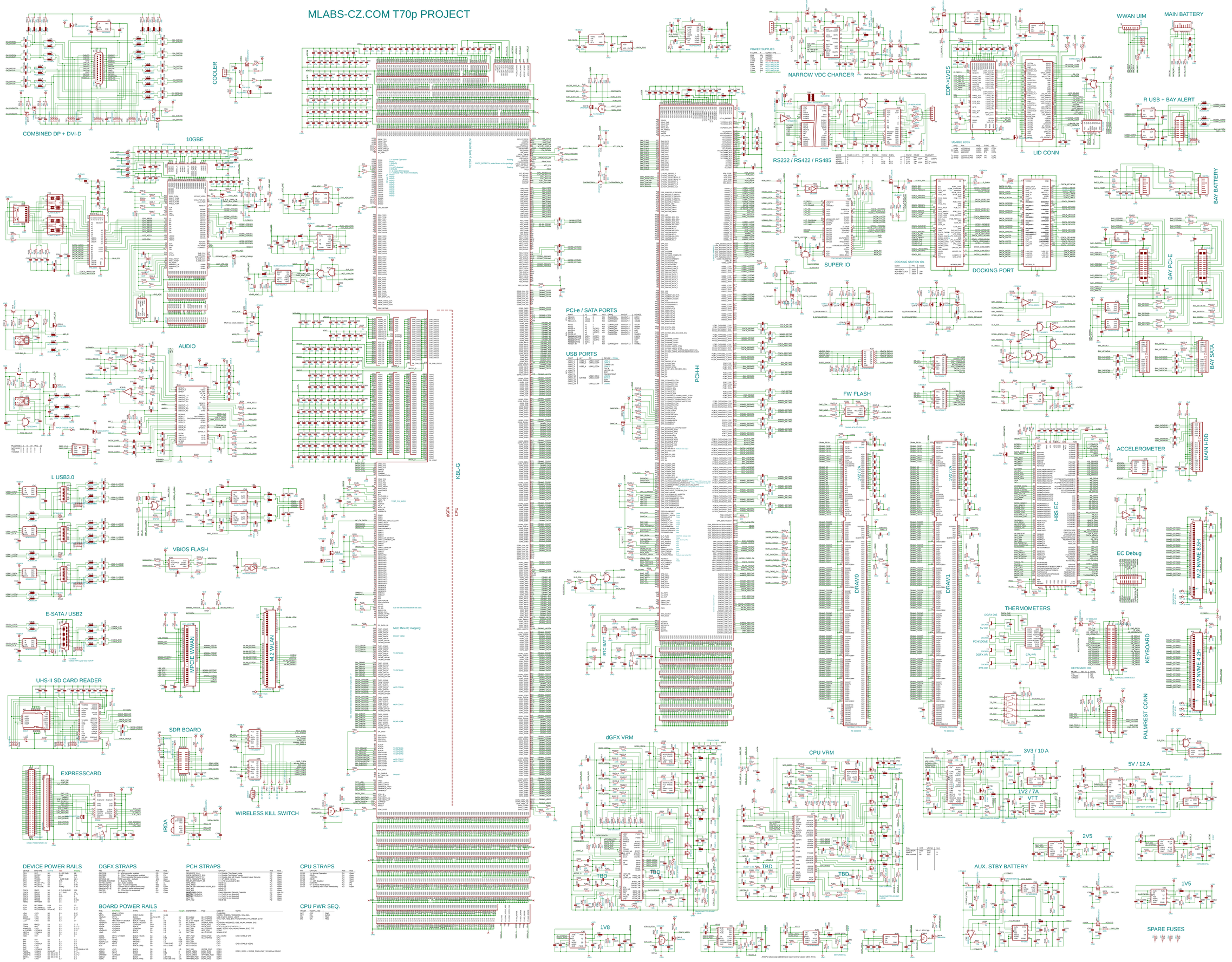
MLABS-CZ.COM T70p PROJECT



DEVICE POWER RAILS

DDR	VDDQ	1.2	0.6	1.3	0.6
CPU	VCCST	0.9	0.5	0.95	0.5
CPU	VCCIO	0.9	0.5	0.95	0.5
CPU	VCCSA	0.9	0.5	1.0	0.5
CPU	VCCIO (PEG)	0.9	0.5	1.0	0.5
CPU	VCCSA (PEG)	0.9	0.5	1.0	0.5
CPU	VCCGT	0.9	0.5	1.3	0.5
DGFX	VDDC	0.9	0.75-0.95 SVID	1.25	
DGFX	VDDCI	0.9	0.7 SVID	0.9	
DGFX	VDDR	0.9	1.8	1.9	
DGFX	VDDR3	0.9	3.3	3.4	
DGFX	VDDIO	0.9	1.8	1.9	
PCH	VCCPRIM_CORE	0.9	1.1	1.2	
PCH	VCCPRIM_1P8	0.9	1.8	2.1	
HDA	+3V3	0.9	3.3	3.37	
HDA	+5V	0.9	5	5.1	
HDA	+5VALW	0.9	5	5.1	
PCH	+3V3	0.9	3.3	3.7	
DDR4	VDD	0.9	1.2	1.2	
DDR4	VPP	0.9	2.5	2.7	
NAND	VCC	0.9	3.3	3.3	
NAND	VCCQ	0.9	1.8	1.8	
SATA	VCCPSUS	0.9	3.3	3.3	
SATA	VCCPHY	0.9	1.1	1.1	
+5V	+5V	0.9	5	5.1	
+3V	+3V	0.9	3.3	3.3	
BAT	VBL	0.9	12	12.6	
BAT	VBLW	0.9	12	12.6	
BAT	VBLALW	0.9	12	12.6	
BAT	VBLALW2	0.9	12	12.6	
DCIN	+DCIN	0.9	19	19.5	
DCIN	+DCIN_P	0.9	19	19.5	
USB3.0	+5VALW	0.9	5	5.1	
USB3.0	+5VALW2	0.9	5	5.1	
USB3.0	+5VALW3	0.9	5	5.1	
ESATA	+5VALW	0.9	5	5.1	
ESATA	+5VALW2	0.9	5	5.1	

DGFX STRAPS

PEG_RXP	1 = Normal Operation	PD	20K
GPIO20	1 = PCIe TX de-emphasis enabled	PD	20K
GPIO22 (S)	1 = Boot BIOS Strap to PCIe port 1	PD	20K
GPIO24 (S)	PCIe lane GPIO	PD	20K
VRDBNDSTRP	1 = Boot BIOS strap to PCIe port 1	PD	20K
GPIO28 (S)	1 = Audio enabled	PD	20K
GPIO33/CPU_STRAP	Unused GPIO pull-down (default)	PD	20K
GPIO35/NC_TF	Unused GPIO pull-down (default)	PD	20K
GPIO52 (S)	1 = Boot BIOS strap to selected SPI	PD	20K
GPIO53	1 = PCIe Gen 3 capable	PD	20K
	Reserved (2)		

PCH STRAPS

SPI_MOSI	Descriptor Override Strap* Header	PU	20K
GSPI0_MOSI/GPP_B18	0 = Disable "No Reboot" mode	PD	Open
GSPI0_CS1/GPP_B23	0 = Enable Intel Platform Trust Technology	PD	Open
GSPI1_MOSI/GPP_B19	0 = SPI BIOS Master	PD	Open
GSPI1_CS1/GPP_B24	0 = Boot BIOS strap selected flash	PD	Open
SPI_MISO	Reserved	PD	Open
SPI_IO2	Reserved	PD	Open
SPI_IO3	Reserved	PD	Open
SPI_WP	Reserved	PD	Open
GPP_B14/GPIO_SUS14	Boot BIOS Destination Override	PD	Open
GPP_B15/GPIO_SUS15	0 = Port 0 is not detected	PD	Open
GPP_B16/GPIO_SUS16	0 = Port 1 is not detected	PD	Open
GPP_B17/GPIO_SUS17	0 = Port 2 is not detected	PD	Open
RSVD (2)	Reserved		

CPU STRAPS

CFG0	1 = Normal Operation	PU	Open
CFG1	RSVD	PU	Open
CFG2	RSVD	PU	Open
CFG3	1 = Enabled	PU	Open
CFG4	1 = Disabled	PU	Open
CFG5	1 = Lowest PCI Express	PU	Open
CFG6	1 = Lowest PCIe Gen Intel/Amd	PU	Open
CFG7	1 = Enabled PCIe Gen Intel/Amd	PU	Open

BOARD POWER RAILS

+5V	+5VALW	S0	5	5.1	1	EC Analog	ALL EXCEPT
+3V	+3VALW	S0	3.3	3.3	1	EC Digital	ALL EXCEPT
+1.5V	+1.5VALT +1.5VSUS	S0	1.5	1.5	11	AC EC Analog	ALL EXCEPT
+1.5V	+1.5VALW	S0	1.5	1.5	1	AC EC Digital	ALL EXCEPT
+1.8V	+1.8VALW	S0	1.8	1.8	1	AC SPI ROM	ALL EXCEPT
+1.8V	+1.8VALW	S0	1.8	1.8	1	AC Fan	ALL EXCEPT
+1.8V	+1.8VALW	S0	1.8	1.8	1	AC SPI_ROM	ALL EXCEPT
+1.8V	+1.8VALW	S0	1.8	1.8	1	AC Fan	ALL EXCEPT
+VCC	VCC	S0	1.0	1	1	MPP_PSD	VDDQ_PSD
+VCC	VCC	S0	1.0	1	1	MPP_PSD	ALL EXCEPT
+VCCP	VCCP	S0	1.0	1	1	MPP_PSD	ALL EXCEPT
+VCCP	VCCP	S0	1.0	1	1	MPP_PSD	ALL EXCEPT
+VCC	VCC	S0	1.0	1.05 SVID	1	ALL EXCEPT	CPU
+VCC	VCC	S0	1.0	0-1.05 SVID	1	ALL EXCEPT	CPU
+VCC	VCC	S0	1.0	1	1	ALL EXCEPT	CPU
+VDDQ	VDDQ	S0	1.2	1.2	1	MPP_PSD	VDDQ_PSD
+VDDQ	VDDQ	S0	1.2	1.2	1	ALL EXCEPT	CPU
+VCCSA	VCCSA	S0	1.0	1	1	ALL EXCEPT	CPU
+VCCSA	VCCSA	S0	1.0	1	1	ALL EXCEPT	CPU
+VCC	VCC	S0	1.0	1.05 SVID	1	ALL EXCEPT	CPU
+VCC	VCC	S0	1.0	0-1.05 SVID	1	ALL EXCEPT	CPU
+VCC	VCC	S0	1.0	1	1	ALL EXCEPT	CPU
+VDDQ	VDDQ	S0	1.2	1.2	1	DGFX_VRIN	VDDQ_PSD